



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,899	09/27/2005	Dong-Gyu Kim	AB-1521 US	4096

32605 7590 07/11/2007
MACPHERSON KWOK CHEN & HEID LLP
2033 GATEWAY PLACE
SUITE 400
SAN JOSE, CA 95110

EXAMINER

HEYMAN, JOHN S

ART UNIT	PAPER NUMBER
----------	--------------

2871

MAIL DATE	DELIVERY MODE
-----------	---------------

07/11/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/550,899	Applicant(s) KIM, DONG-GYU	
	Examiner John Heyman	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>09/27/2005</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 09/27/2005 was filed after the mailing date of the instant application on 09/27/2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto (US 2002-182766, cited in the IDS herein). Looking at Fig. 1 of Yamamoto and comparing it with Claim 1, the gate electrode, gate insulating layer, semiconductor layer, data line/source electrode, drain electrode, color filter, opening to drain electrode, light blocking layer on the color filter, passivation layer with contact hole, pixel electrode and spacer recited are seen respectively anticipated by gate electrode 102, gate insulating layer 103, semiconductor layer 104, data-line/source electrode 105, drain

Art Unit: 2871

electrode 106 (interchangeably labeled as a source electrode in Yamamoto), color filter 108, opening in color filter 108, light blocking layer 109, passivation layer 110 which has a contact hole 111, pixel electrode 112 and spacer 113. The limitations of Claims 2 and 3 are met by paragraphs 53 and 55 wherein Yamamoto discloses that his light blocking layer 109 and spacer 113 are made of resin, an organic material. Yamamoto discloses that his passivation layer 110 is made of an acrylic material in para. 54 to meet Claim 9, and that semiconductor layer 104 is seen in Fig. 1 as having the same planar shape as the data lines and drain electrodes as recited in Claim 10. Regarding Claims 11 and 12, the first panel includes a gate line inherently part of the gate electrode 102, a data line 105 which shows a thin film transistor formed therewith, a pixel electrode 112 connected to the TFT, and a light blocking layer 109 made of organic material, while the second panel facing the first panel includes a common electrode 212 and spacer 113 forming a gap with the first panel as recited in Claim 11. The color filter of Claim 12 is shown by color filter 108 formed on the first panel (of Claim 11) and has an opening exposing the drain electrode 106 at least in part as recited.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto as applied to claims 1-3 above, and further in view of Rho et al (Rho - US 6,862,050). What is not shown in Yamamoto are the details of a storage conductor in combination with a TFT formed under the gate insulating layer and at an opening made through the color filter/passivation layers. Looking at Fig. 3, for example, in Rho, a storage conductor 30 is shown in combination with a TFT formed under gate insulating layer 40 overlapping a gate line 21 (Fig. 2) and electrically connected to pixel electrode 140 to meet Claim 4. The second opening of Claim 5 is seen as contact hole 120 in Rho, which exposes in part storage conductor 30 to pixel electrode 140 as recited. In Claims 6-8, again, the storage conductor is storage conductor 30, which is seen formed under gate insulating layer 40 and overlapping the pixel electrode 140 as recited. Thus, it would have been obvious under 35 USC 103 to provide a storage conductor and opening arrangement as shown by Rho in Yamamoto for the reason given in Rho, namely, to increase the storage capacitance, a well known and desirable feature for liquid crystal displays. That is, to employ a well known and desirable feature in a well known manner (Rho) to the prior art (Yamamoto) would not be patentable since the motivation is clearly taught by the prior art (Rho).

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto as applied to claim 11 above, and further in view of Lee et al (Lee US 6,535,259). See Fig. 5, for example of Lee, which shows protrusion 90 formed on one of two opposing substrates with slanted lateral surfaces as recited. It would have been

Art Unit: 2871

obvious under 35 USC 103 to apply the teaching of Lee in Yamamoto for the reason given in Lee, namely, to obtain a wide viewing angle and a fast response time (by controlling the orientation of the liquid crystal molecules) in a liquid crystal display. See col.1 line 8.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakata et al. and Sakamoto et al. are cited to show LCDs having many of the features claimed herein. These references should be carefully reviewed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Heyman whose telephone number is 571 272-5730. The examiner can normally be reached on 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571- 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2871

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSH


ANDREW SCHECHTER
PRIMARY EXAMINER